AMENDMENT TO THE CLAIMS:

1. (Cancelled)

2. (Currently amended) The digital signal processor as defined in ~~claim 1,~~ claim 4, wherein

~~the~~ said auxiliary arithmetic device has a priority judgment circuit ~~for determining the~~ operable to determine a priority for performing the processing of the demanded task, ~~for which the processing is demanded,~~ to execute the processing, and

~~the~~ said auxiliary arithmetic device ~~performs~~ is operable to perform the demanded task in accordance with the priorities of respective tasks determined by ~~the~~ said priority judgment circuit.

3. (Currently amended) The digital signal processor as defined in ~~claim 1,~~ claim 4, wherein

~~the~~ said auxiliary arithmetic device has an interruption signal generation circuit ~~for generating~~ operable to generate an interruption signal interrupting ~~the~~ processing which is under execution, and

when receiving the task demand from ~~the~~ said main arithmetic device, ~~the~~ said auxiliary arithmetic device interrupts the processing which is under execution and performs the demanded task. ~~task demanded from the main arithmetic device.~~

4. (New) A digital signal processor comprising:

a main arithmetic device operable to generate a task demand; and

an auxiliary arithmetic device operable to receive the task demand from said main arithmetic device and to perform a demanded task, which corresponds to the task demand,

wherein said auxiliary arithmetic device comprises a program memory area having a task list stored therein a reservation processing register and a clear circuit,

wherein said program memory area includes previously stored therein, a plurality of tasks that are to be processed by said auxiliary arithmetic device in a prescribed cycle, and an interrupt task which is to be executed in accordance with the task demand,

wherein said task list defines an order in which the plurality of tasks stored in said program memory area are to be processed by said auxiliary arithmetic device,

wherein said reservation processing register is operable to set the task demand from said main

arithmetic device even when said auxiliary arithmetic device is processing the plurality of tasks,

wherein said clear circuit is operable to clear the task demand in said reservation processing register after the interrupt task corresponding to the task demand set in said reservation processing register is executed, and

wherein said auxiliary arithmetic device is operable to execute the interrupt task corresponding to the task demand from said main arithmetic device only once, after terminating processing of one of the plurality of tasks.